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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,881	02/12/2002	Jiann-Tyng Tzeng	TS01-617	6517

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,881 ✓	TZENG ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,12-18,23 and 33-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,12-17 and 33-36* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 33 – 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (USPAT 6143579, Chang).

With regard to claims 33 and 34, Chang discloses in the abstract and column 1, lines 19 – 36 a method for monitoring electron charge effect occurring during semiconductor processing. Chang discloses in figures 1 – 4 forming a monitor wafer (10) having floating gate structures (16). It should be noted that the term "monitor" is an intended use recitation for the wafer, and that the gate structures 16 of Chang meet the floating gate limitation of the claimed invention. Chang discloses in the abstract and column 6, lines 35 – 53 exposing the monitor wafer to a plasma process. Chang discloses in the abstract, column 4, lines 14 – 31, and column 6, line 35 – column 7, line 11 measuring plasma damage by measuring interlayer oxide electron trap out rate comprising measuring a voltage required to induce a FN tunneling based current between at least one contact point of said floating gate structures and said monitor wafer. It should be noted that the measuring step is an intended use recitation that bears no patentable weight in a method of making claim.

With regard to claim 35, it should be noted that the claim limitation "the FN tunneling based current between at least one contact point of said floating gate structure and said monitor wafer being about 0.1 μA" is an intended use recitation.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 5, 12 – 17 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Yang (USPAT 5913102) and Ahn (USPAT 5563080).

With regard to claim 1, Chang discloses in the abstract and column 1, lines 19 – 36 a method for monitoring electron charge effect occurring during semiconductor processing. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 providing a substrate (10), a layer of conductivity having been created in the substrate. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 that the layer of conductivity created in the surface of the substrate is p-type. Chang does not disclose that the layer of conductivity created in the surface of the substrate is n-type. Yang discloses in figure 2, and column 6, lines 37 – 39 providing a substrate (20), a layer of n-type conductivity having been created in the surface of the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the n-type conductivity layer of Yang in the method of Chang in order to use an alternatively doped

substrate as appropriate for a given process as is well known in the art. Switching conductivity type is well known to be obvious in the art depending on the specific types of devices being fabricated. Chang discloses in figure 1 and column 5, lines 17 – 28 creating a pattern of Local Oxidation of Silicon (LOCOS) regions (12) in the substrate, the pattern of LOCOS being interspersed with exposed regions (8) of the substrate. Chang does not disclose etching the exposed regions of the substrate using the pattern of LOCOS regions as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. Ahn discloses in figures 3b – 3c etching exposed regions (17) of a substrate (11) using a pattern of LOCOS regions (16) as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching with LOCOS regions as hard masks of Ahn in the method of Chang and Yang in order to improve integration of a semiconductor device by preventing junction breakdown from occurring as stated by Ahn in column 4, lines 11 – 14. Chang discloses in figure 1 and column 5, line 28 creating a layer of interlayer oxide (14) over the pattern of LOCOS regions and the inside surfaces of the trenches created in the substrate. Chang discloses in figure 1, and column 5, lines 30 – 32 depositing a layer of polysilicon (16) over the layer of interlayer oxide. Chang discloses in figures 2a and 2b patterning (18) the layer of polysilicon, the patterned layer of polysilicon comprising at least one contact point over the substrate, completing creation of a electron charge monitoring device having a surface. Chang discloses in the abstract and column 6, lines 35 – 37 providing a semiconductor processing tool, the semiconductor processing tool being designated as being a tool being evaluated for electron charge effect of a process being performed by the tool. Chang

discloses in the abstract and column 6, lines 35 – 53 positioning the substrate comprising the electron charge-monitoring device inside the processing tool in a location and a position being occupied by a substrate being processed by the tool. Chang discloses in the abstract and column 6, lines 35 – 53 establishing processing conditions of a process as these processing conditions apply for the process and the tool. Chang discloses in the abstract and column 6, lines 35 – 58, exposing the electron charge monitoring device to the established processing conditions for a period of time. Chang discloses in the abstract and column 6, lines 54 – 58 terminating the processing conditions. Chang discloses in the abstract and column 6, line 60 removing the electron charge monitoring device from the semiconductor processing tool. Chang discloses in the abstract, column 4, lines 14 – 31, and column 6, line 35 – column 7, line 11 measuring voltage required to induce a FN tunneling based current between the at least one contact point of the patterned layer of polysilicon and the substrate. It should be noted that the measuring a voltage step is an intended use recitation that bears no patentable weight in a method of making claim.

With regard to claim 13, Chang discloses in the abstract and figures 1 – 2b a method of creating an electron charge effect monitoring device. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 providing a substrate (10), a layer of conductivity having been created in the substrate. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 that the layer of conductivity created in the surface of the substrate is p-type. Chang does not disclose that the layer of conductivity created in the substrate is n-type. Yang discloses in figure 2, and column 6, lines 37 – 39 providing a substrate (20), a layer of n-type conductivity having been created in the substrate. It would have been obvious to one of ordinary skill in the art at the

time of the present invention to use the n-type conductivity layer of Yang in the method of Chang in order to use an alternatively doped substrate as appropriate for a given process as is well known in the art. Switching conductivity type is well known to be obvious in the art depending on the specific types of devices being fabricated. Chang discloses in figure 1 and column 5, lines 17 – 28 creating a pattern of Local Oxidation of Silicon (LOCOS) regions (12) in the substrate, the pattern of LOCOS being interspersed with exposed regions (8) of the substrate. Chang does not disclose etching the exposed regions of the substrate using the pattern of LOCOS regions as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. Ahn discloses in figures 3b – 3c etching exposed regions (17) of a substrate (11) using a pattern of LOCOS regions (16) as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching with LOCOS regions as hard masks of Ahn in the method of Chang and Yang in order to improve integration of a semiconductor device by preventing junction breakdown from occurring as stated by Ahn in column 4, lines 11 – 14. Chang discloses in figure 1 and column 5, line 28 creating a layer of interlayer oxide (14) over the surface of the pattern of LOCOS regions and the inside surfaces of the trenches created in the substrate. Chang discloses in figure 1, and column 5, lines 30 – 32 depositing a layer of polysilicon (16) over the layer of interlayer oxide. Chang discloses in figures 2a and 2b patterning (18) the layer of polysilicon, the patterned layer of polysilicon comprising at least one contact point over the substrate. Chang discloses in the abstract, column 4, lines 14 – 31, and column 6, line 35 – column 7, line 11 measuring a voltage required to induce a FN tunneling based current between the at least one contact point of the

patterned layer of polysilicon and the substrate after the substrate has been exposed to a semiconductor processing tool under known conditions of processing by the semiconductor processing tool. It should be noted that the measuring a voltage step is an intended use recitation that bears no patentable weight in a method of making claim.

With regard to claims 2 and 14, Chang discloses in figure 1 and column 5, lines 17 – 27 creating a pattern of Local Oxidation of Silicon (LOCOS) regions in the substrate. Chang discloses in column 5, lines 20 – 22 depositing a layer of silicon nitride over the surface of the substrate. Chang discloses in column 5, lines 20 – 22 patterning the layer of silicon nitride, creating a mask of silicon nitride over the substrate, elements of the mask being interspersed with exposed regions of the substrate. Chang discloses in figure 1 and column 5, lines 17 – 27 creating layers of Local Oxidation of Silicon (LOCOS) in the exposed regions of the substrate. Chang discloses in figure 1 and column 5, lines 17 – 27 removing the mask of silicon nitride from the substrate. While Chang discloses that the LOCOS process is used, Ahn teaches other details of this well known process in figures 3a – 3c and column 2, line 52 – column 3, line 5.

With regard to claim 3 and 15, Chang discloses in column 5, lines 28 – 30 wherein the layer of interlayer is dry oxide.

With regard to claims 4 and 16, Chang discloses in column 5, lines 28 – 30 the layer of interlayer oxide being created to a thickness of 190 Angstrom.

With regard to claims 5 and 17, Chang discloses in column 5, lines 32 – 34 the layer of polysilicon being deposited to a thickness within the range of about 1,500 and 6,000 Angstrom (3,750 Angstrom reads on the claimed range).

With regard to claim 12, it should be noted that the claim limitation "the current induced between the layer of polysilicon and the substrate being about 0.1 μA" is an intended use recitation. Therefore, Chang, Yang, and Ahn read on this limitation.

With regard to claim 36, Chang discloses in the abstract and column 1, lines 19 – 36 a method for monitoring electron charge effect occurring during semiconductor processing. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 providing a monitor substrate (10) having a layer of conductivity therein. Chang discloses in figure 1, and column 4, line 66 – column 5, line 27 that the layer of conductivity created in the surface of the substrate is p-type. Chang does not disclose that the layer of conductivity created in the surface of the substrate is n-type. Yang discloses in figure 2, and column 6, lines 37 – 39 providing a substrate (20), a layer of n-type conductivity having been created in the surface of the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the n-type conductivity layer of Yang in the method of Chang in order to use an alternatively doped substrate as appropriate for a given process as is well known in the art. Chang discloses in figure 1 and column 5, lines 17 – 28 including oxidized regions formed over the conductivity and interspersed with exposed regions (8) of the substrate. Chang does not disclose that the interspersed regions are trench regions that each include an opening extending into said monitor substrate. Ahn discloses in figures 3b – 3c oxidized regions (16) formed over a monitor substrate (11) and interspersed with trench regions (17) that each include an opening extending into the monitor substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the trench regions of Ahn in the method of Chang and Yang in order to improve integration of a semiconductor device by preventing junction breakdown from occurring

as stated by Ahn in column 4, lines 11 – 14. Chang discloses in figure 1 and column 5, line 28 an interlay oxide (14) layer disposed over the oxidized regions. It is further obvious in the method of Chang, Yang and Ahn that the interlayer oxide layer would be disposed over the oxidized regions and the trench regions. Chang discloses in figure 1, and column 5, lines 30 – 32 a patterned polysilicon layer (16) disposed over said interlayer oxide Layer and comprising at least one contact point over said monitor substrate that forms an electron charge monitoring device having a surface. Chang discloses in the abstract and column 6, lines 35 – 37 providing a semiconductor-processing tool designated as being evaluated for electron charge effect of a process being preformed by said semiconductor processing tool. It should be noted that it is inherent that a plasma etcher would need evaluation. Chang discloses in the abstract and column 6, lines 35 – 53 positioning said monitor substrate inside said semiconductor-processing tool in a Location and a position generally occupied by a substrate being processed said semiconductor-processing tool. Chang discloses in the abstract and column 6, lines 35 – 53 establishing processing conditions for said process. Chang discloses in the abstract and column 6, lines 35 – 58 exposing said electron charge Monitoring device to said established processing conditions for a period of time. Chang discloses in the abstract and column 6, line 60 removing the electron charge-monitoring device from the semiconductor-processing tool. Chang discloses in the abstract, column 4, lines 14 – 31, and column 6, line 35 – column 7, line 11 measuring a voltage required to Induce a FN tunneling based current between the at least one contact point of said patterned layer of polysilicon and said monitor substrate. It should be noted that the measuring a voltage step is an intended use recitation that bears no patentable weight in a method of making claim.

Allowable Subject Matter

5. Claims 6 and 18 are allowed.

6. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed August 24, 2004 have been fully considered but they are not persuasive.

8. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

9. In response to applicant's argument that measuring the wafer for Q_{BD} and E_{BD} is substantially different than measuring the FN tunneling current, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and

the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

10. With regard to applicant's argument that "The processes of FIGs. 4 – 10 and 11 are both believed to be novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skill in the art," it should be noted that the Figures are not what defines a patentable invention. The claims define the invention. In this case it has been determined that the "various references" do provide a sufficient basis for "concluding that the combination of claimed elements" are not obvious to one of ordinary skill in the art. Applicant has provided no reasons why the specific motivations for the combinations might fail. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II